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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,121	04/09/2004	Phong N. Nguyen	MI22-2557	2457

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EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 02/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,121	NGUYEN, PHONG N.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 62-74 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 62-74 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to the Amendment filed on 11/9/2004.

Currently, claims 62-74 are pending.

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 62-74 are rejected under 35 U.S.C. 103(a) as being obvious over Applicant's Admitted Prior Art of Record (filed 4/09/2004) in view of Pfiester et al. (U.S. Patent No. 4,984,042 patented 1/8/1991).

The Applicant's Admitted Prior Art of record shows the method substantially as claimed in Figs. 1-6 and corresponding text as: a semiconductive material substrate (12)(Fig. 1) ([0005], pg. 2 , lines 2-3); a pair of partially-formed adjacent transistor gates (30,32) over the semiconductor substrate, the partially-formed transistor gates each having a lowermost layer of conductive material (16) therein, the lowermost layer of conductive material of one of the partially-formed transistor gates being a first segment of conductive material and the lowermost layer of conductive material of the other partially-formed transistor gate being a second segment of conductive material (Fig. 2)([0012], pg. 4, lines 1-6); a third segment of conductive material (the part of (16) that lies between 30 and 32) extending between the partially-formed adjacent transistor gates and from the first segment of conductive material to the second segment of conductive material (Fig. 2)([0012], pg. 4, lines 1-6); and at least one conductively-doped region (48) within the substrate 12 ([0017], pg. 5, lines 1-7) (Claim 62). The Admitted Prior Art teaches that at least one conductively-doped diffusion regions (68,70), extends to under at least one of the partially-formed adjacent transistor gates (Fig. 5) ([0022], pg. 6, lines 1-8)(claim 63). The Admitted Prior Art teaches that the first, second and third segments of conductive material consist of conductively-doped silicon ([0007], pg. 2-3, lines 1-6) (claim 64). The Admitted Prior Art teaches that a pad oxide layer (14) ([0006], pg. 2 lines 1-2) is formed beneath the partially-formed transistor gates and beneath the first, second and third segments (Fig. 2) ([0007] pgs. 2-3, lines 1-6), and wherein each of the partially-formed transistor gates further comprises; at least one additional layer of conductive material (18, 20) over the first and second segments

of the conductive material (Fig. 2)([0008], pg. 3, lines 1-5); and an insulative layer (22) over the at least one additional layer of conductive material (Fig. 2) ([0009], pg. 3, lines 1-4) (claim 65). The Admitted Prior Art teaches that the additional layer of conductive material comprises a layer of tungsten over a layer of tungsten nitride ([0008], pg. 3, lines 1-5) (claim 66). The Admitted Prior Art teaches that the insulative layer comprises silicon nitride ([0009], pg. 3, lines 1-4)(claim 67). The Applicant's Admitted Prior Art of record shows the method substantially as claimed in Figs. 1-6 and corresponding text as: a semiconductive material substrate (12)(Fig. 1) ([0005], pg. 2, lines 2-3); a conductive layer (16) over the substrate, the conductive layer having a thin segment between a pair of thicker segments, one of the thicker segments being a first thicker segment and the other being a second thicker segment (Fig. 2) (Fig. 2)([0012], pg. 4, lines 1-6); a first gate stack (30) over the first thicker segment and a second gate stack (32) over the second thicker segment, the first and second gate stacks being spaced from one another by a gap extending over the thin segment (Fig. 2) ([0012], pg. 4, lines 1-7) ([0013], pg. 4, lines 1-3); the first and second gate stacks comprising one or more conductive materials (18,20) over the thicker segments and comprising one or more insulative materials (22) over the one or more conductive materials (Fig. 2) ([0008], pg. 3, lines 1-5) ([0009], pg. 3, lines 1-4); and at least one conductively-doped region 48 within the substrate ([0017], pg. 5, lines 1-7) (Claim 68). The Admitted Prior Art teaches that one or more insulative layers include a layer comprising silicon nitride ([0009], pg. 3, lines 1-4) (claim 69). The Admitted Prior Art teaches that one or more conductive materials comprise a layer of tungsten over a layer of tungsten nitride ([0008], pg. 3,

lines 1-5) (claim 70). The Admitted Prior Art teaches that the thin segment has a thickness of about 100/ to about 400/ (Fig. 2) ([0010], pg. 3-4, lines 1-15) ([0012], pg. 4, lines 1-7)(claim 71). The Admitted Prior Art teaches a masking material (60) formed over the first and second gate stacks, the masking material having an opening extending to the at least one conductively-doped region ([0020], pg. 6, lines 1-4) ([0021], pg. 6, lines 1-11) (claim 72). The Admitted Prior Art teaches that at least one conductively-doped region includes at least one region, which extends to under at least one of the first and second gate stacks (Fig. 5) ([0022], pg. 6, lines 1-8) (claim 73). The Admitted Prior Art teaches that the conductive layer consists of conductively-doped silicon ([0007], pg. 2-3, lines 1-6) (claim 74).

The Admitted Prior Art lacks anticipation only in not explicitly teaching that: 1) one or more conductively-doped diffusion regions within the substrate and directly under the third segment; at least one of said one or more diffusion regions extending from said one of the partially-formed transistor gates to said other of the partially-formed transistor gates (claim 62) 2) at least one conductively-doped region within the substrate is directly under the third or thin segment (claim 68); and 3) a masking material formed over the first and second gate stacks, the masking material having an opening extending therethrough to the thin segment (claim 72).

Pfiester teaches, in a similar transistor device, where the substrate is implanted through a conductive layer (17) to form a conductively-doped region (col. 3, lines 27-57). The implant is carried out to improve the process for making integrated circuits (col. 2, line 7-10). One such improvement is, the polysilicon layer bleeds off charge that is

developed by implanting. Another advantage is that the oxide layer is protected from being damaged by the implant (col. 4, lines 23-50). In the process of implanting, the conductive layer (polysilicon) may be combined with a mask having an opening prior to implantation (col. 3, lines 27-57).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method shown in The Admitted Prior Art, by implanting the substrate to form the conductively-doped region through the conductive layer (polysilicon) as taught in Pfiester, with the motivation that this will provide an improved structure and provide an improved process for forming integrated circuits, by allowing charge accumulated during an implant to be bled off by the conductive layer. Additionally the conductive layer protects the underlying oxide layer from being damaged by the implant.

Response to Arguments

5. Applicant's arguments filed 11/09/2004 have been fully considered but they are not persuasive. While it is noted that Pfiester does not thin the conductive layer, when the teachings of Pfiester, where implants into the substrate through a conductive layer occur, are combined with the Admitted Prior Art does do to the fact that Fig. 3 shows a thinned conductive layer that can be implanted through. This combination of the Admitted Prior Art and the teaching of Pfiester where the implantation occurs through a conductive layer in the examiner's view still reads on claim 68, and as such remains rejected. Also the examiner views the addition of one or more conductively-doped diffusion regions does not overcome the present rejection.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WLL
January 26, 2005

MICHAEL S. LEBENTRITT
PRIMARY EXAMINER